FULL SMT 38 GHz INTEGRATED RADIO FOR POINT TO POINT LOW CAPACITY LINKS

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Abstract: This paper deals with the innovative integration technology adopted for the development of the highest frequency implementation, namely at 38 GHz, relevant to a new PDH family radio. In particular this radio solution copes with severe market requirements such as low cost equipment, mass production, short delivery time and ETSI standard compliance. All the above targets have been reached using a very compact design approach, standard SMT assembly process (even up to 38 GHz), and state of the art Microwave MW devices. Technology aspects, technical solution and testing strategy along with test results and then detailed.

Keywords: 5–10 Digital Equipment (for) telecommunication system (using) integrated circuit package design.

1. INTRODUCTION

As it has been mentioned in the abstract paragraph, this radio belongs to a new PDH radio family for Point to Point system covering several frequency bands (from 13 to 38 GHz) and able to support data rate from 4xE1 to 16xE1 in accordance with ETSI Standard requirement EN 302 217-2-2 .
The product is intended to be used both for cellular networks infrastructure and Transport wireless backhaul (fixed Point to Point links). Precisely the system is a split radio consisting of Indoor Unit IDU containing Base Band Mux and Demux and of an ODU equipment containing both the MW and Modem circuits; An aggregate at 51.84 Mb/s, travelling on the IDU-ODU interconnection cable, transports up to 16xE1 data fluxes and the appropriate signalling interface.
The remarkable benefits, related to the new product, have to be found in the very compact ODU design HW architecture in which all the core radio functions: MW Transceiver, Modem unit and cable interface are integrated in a multi-layer single board using standard SMT assembly. Because of the integrated design approach, reduced number of test points and of a unique ATE station (common to all the frequency bands), the overall ODU design results compatible with low cost goal, mass production process and short delivery time.

2. OUTDOOR UNIT ARCHITECTURE

The most challenging ODU development was the 38 GHz Band due to the severe HW design constraints (common to the other frequency implementations): single board design, multifunction MMIC usage and integration of bare dies in low cost SMD packages. A simplified block diagram of the ODU unit is shown in fig. 1 whilst a mechanical break-down is shown in fig. 2. and relevant ODU cabinet in fig. 3
With reference to fig. 1, the ODU architecture consists of a cable interface to process Traffic Data, TLM/TLC signals and dc supply, of a dc supply unit (including DC/DC converter and power distribution), of a digital Modem, of an Rx/Tx section (including I-Q mixers) and of a MW Transceiver (including Tx, Rx and MW synthesizer). All the above parts are integrated in the MW/Modem board. A waveguide diplexer connects the Tx and Rx ports to the Antenna interface. Main performance of the 38 GHz radio are reported in Table 1.
The ODU is completely programmable by the IDU or by a local control terminal to allow the final automatic tuning procedure.

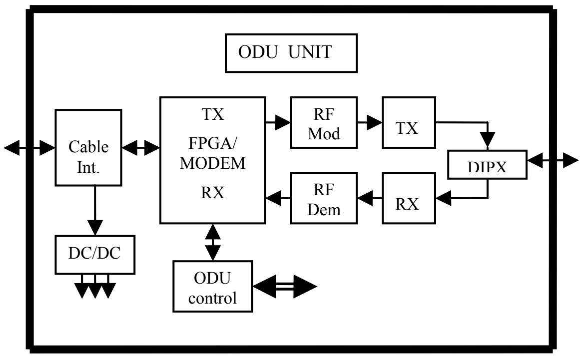

Fig. 1 ODU Block Diagram.

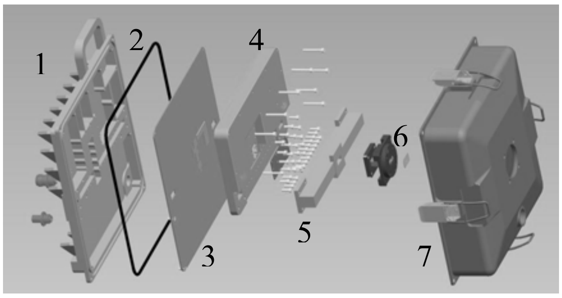

Fig. 2 ODU mechanical break-down: 1 – Base plate and heat sink, 2 – Gasket, 3 – MW-Modem PCB, 4 – PCB Cover, 5 – Diplexer, 6 – Adapter, 7 – Top Cover

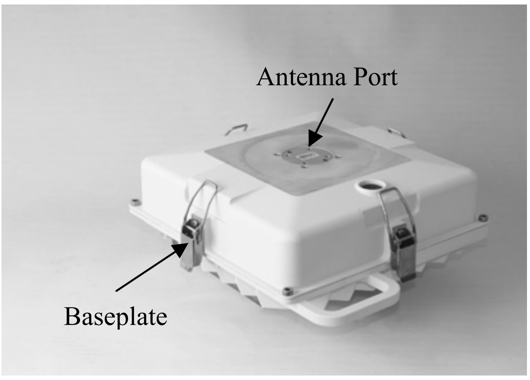

Fig. 3 ODU Cabinet

Table 1 – 38 GHz ODU Performance

Frequency Range	37 ÷ 39.5 GHz
Nominal Tx Power	17 dBm
Tx Power Range	20 dB
Rx NF	7 dB
RX threshold BER @ 1E-3 2xE1	-89 dBm
RX threshold BER @ 1E-3 8xE1	-83 dBm
RX threshold BER @ 1E-6 2xE1	-87.5 dBm
RX threshold BER @ 1E-6 8xE1	-81.5 dBm
ETSI Standard	EN 302 217-2-2

3. MICROWAVE/MODEM SINGLE BOARD

The Radio architecture is a canonical one; conversely the innovative concept is the HW technological development used up to 38 GHz. In particular the most efforts have been focused in integrating all the electronic parts in only one PCB designing a complex multilayer build-up, using multifunction MW Integrated circuits, concentrating the Modem DSP and control loops in a dedicated FPGA and using a full SMT assembly process.
The choice to put all the radio parts in a single Board was also due to cost reduction targets. In fact most of the savings comes from the removal of external interfaces and interconnection circuits, mechanical shielding and reduction of testing steps. The MW/Modem functional block diagram is shown in fig. 4.
With reference to the functional architecture (fig. 4), the unit can be divided into two subsections, a digital/base band part which sends/receives data to/from the IDU, and an analog/MW part which send/receives an RF modulated signal to/from the antenna.
In details Data (payload and communication channel) from and to the IDU, contained in a bidirectional aggregate Base Band signal, are separated by a cable electrical interface and by a FPGA/MODEM. The payload coming from the IDU (from 2xE1 to 16xE1) is modulated in a CPM modulation format, and sent to the MW TX output of the board. The extraction of the payload from the aggregate and the generation of I/Q base band signals are performed by the FPGA/MODEM. The conversion of the base band signal to radio frequency is performed by a direct 19 GHz modulator, followed by a frequency doubler, by a level control circuit and a power amplifier.
The radio signal received at the MW RX input is demodulated and the extracted payload is sent to the IDU. Namely the radio frequency signal is down converted to an intermediate frequency equal to the shift, and then demodulated to I/Q base band signals. The FPGA/MODEM, then, extracts the payload from the base band signal and inserts it in the aggregate sent to the IDU. Commands and configuration coming from the IDU are executed by an ODU microcontroller, which also sends measurements and alarms to the IDU. A set of DC/DC converter generates the internal positive and negative supplies from the -48V supply coming from the IDU.

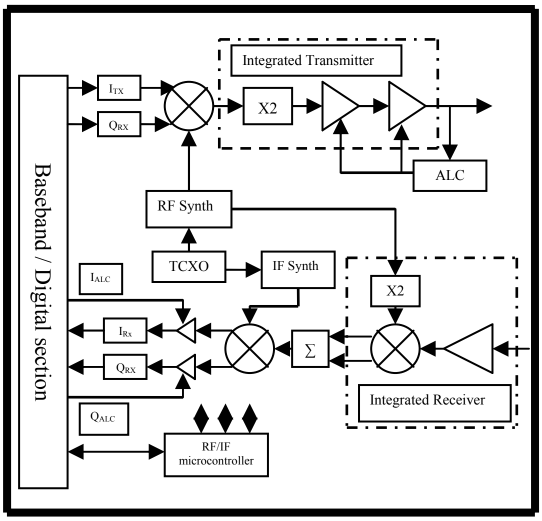

Fig. 4 MW/Modem functional block diagram

3.1 PCB Build-up and integration architecture

The single Board (Fig. 5) build-up consists of a 8 dielectric layers structure; the first and fourth layers are made of Rogers material RO 4350, the others are standard epoxy resin material (FR4 similar). The top layer is made of Rogers substrate because it supports the MW signals.. The routing of DC , IF and digital signals are performed both on the top and the inner layers by the use of microvias; on the contrary the MW signals travel only on the top layer. The MW waveguide cavities are directly machined in the PCB assembly using high accuracy mechanical process; relevant ground planes are obtained either metallizing the cavities walls or by the use of blind vias dense arrays; waveguide input/output return loss resulted better than 15 dB.

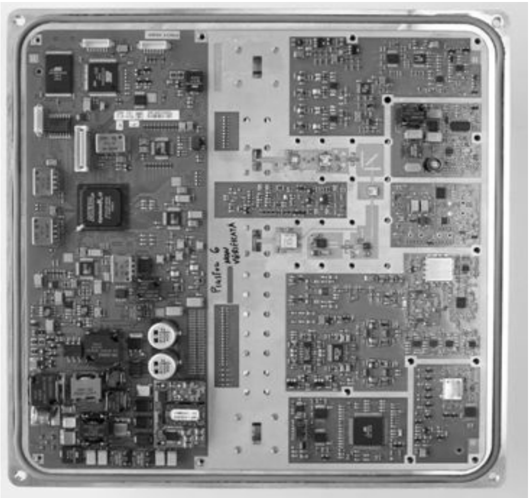

Fig. 5 MW/Modem PCB

3.2 Microwave section

The MW Transceiver section (see detail in Fig. 6) utilizes a full SMT chipset; in particular of a HBT VCO, working around 19 GHz (locked to a crystal reference) to generate carrier signal to the TX chain ad LO drive to RX down converter, of an integrated Receiver, of a TX I-Q Mixer (working around 19 GHz) and of a TX Power Doubler to provide TX output carrier at 38 GHz.

The receiver integrates four functions onto one chip: an LNA, which provides the optimum noise figure; an image reject mixer with high linearity performance; an LO driver amplifier; and a frequency doubler for the LO input. The image reject mixer eliminates the need for a bandpass filter after the LNA to remove thermal noise at the image frequency. I and Q mixer outputs are provided, and an external 90-degree hybrid is required to select the desired sideband. The integrated LO buffer amplifier reduces the LO power requirement. Fig. 7 shows the an image of the packaged receiver with the lid removed. The transmitter power device (see Fig. 8) combines an active frquency doubler with an output buffer amplifier that delivers up to +25 dBm output power and has an excellent harmonic rejection including the fundamental. It is enclosed in a 7 mm x 7 mm air cavity package (see Bessemoulin A., et all, 2004 and Van Hejiningen et All 2004). Both the transmitter and receiver MMICs are equipped with ESD protection circuits (see Bessemoulin A., et all, 2006) to improve reliability during SMT assembly process.

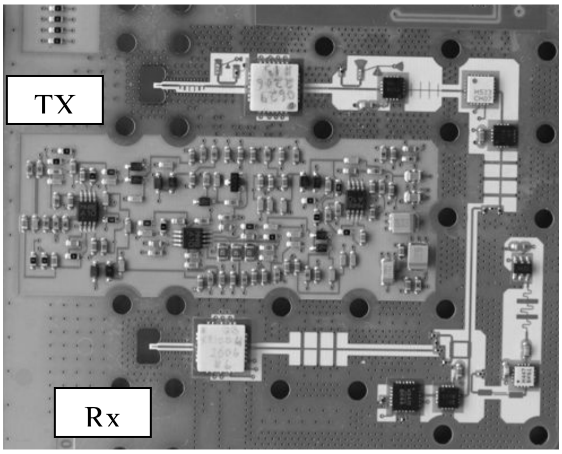

Fig. 6 MW/Modem functional block diagram. This block includes an RF VCO followed by branch line hybrid to LO drive both the Tx and Rx chains. The Rx part is shown in the picture lower side whilst the Tx part in the upper side

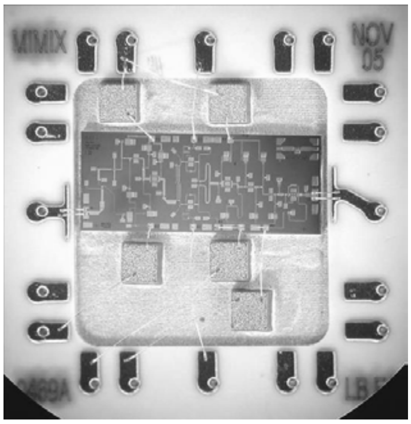

Fig. 7. MMIC Integrated receiver in the package with lid removed and bonding arrangements. Courtesy of Mimix Broadband Inc.

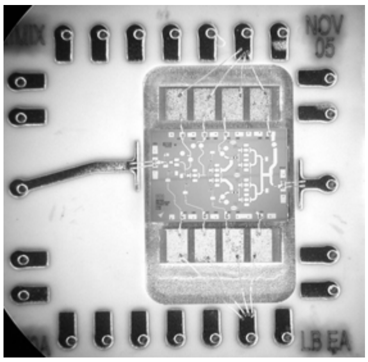

Fig. 8. MMIC Integrated frequency doubler in the package with lid removed and bonding arrangements - Courtesy of Mimix Broadband Inc.

The transmitter side I-Q modulator is a compact MMIC device using a pair of double balanced mixers and 90° hybrid fabricated in GaAs MESFET process and packaged in a standard plastic leadless assembly. The device shows an image rejection better than 20 dBc and LO-RF isolation better than 40 dB. With the use of an external feedback circuit based on envelope detector method, image and LO suppression result better than 40 dB in the overall 38 GHz bandwidth. The RF synthesizer consists of an HBT MMIC VCO, see (Kaneko T., et all, 2000), working around at 19 GHz, locked to a quartz reference by a PLL circuit having 3 dB bandwidth below 1 KHz. Phase Noise performance is better than 85 dBc at 100 KHz carrier offset. Because the RF synthesizer generates a single source driving the RF I-Q mixer, the received IF frequency is the same of the frequency shifter (Tx / Rx frequency spacing); in the 38 GHz application the IF frequency is 1260 MHz. All the IF chipset (Rx I-Q, VCO, IF amp stages…) are COTS devices using standard SMT plastic packages.

3.3 Modem section

The modulation format is four level continuous phase modulation. The phase impulse shape is raised cosine and the length is two symbols. In literature this scheme is synthetically defined 4CPM 2RC.
The modem is an evolution of the one described by (Lankl and Loeckel, 1996) and (Lankl, *et al*., 1996). An advanced differential detection (Lankl and Friederichs 1995; Spinnler, *et al*. 1999) makes the modem very robust against frequency jumps with negligible penalty in the BER curve.
Many functions are fully digitally implemented: multi-rate digital filters, AFC (automatic frequency control), CMA (constant modulus algorithm) equalizer, modulation error compensation, cable interface, framer. The complete digital part of the modem is housed in a low cost FPGA. The modem can be upgraded for improved functionality or bug fixing by software download.

3.4 Assembly and Test procedure

The entire equipment test process can be divided into the following steps:
AOI/ICT Test: In the first step it is performed an Automated Optical Inspection and an In Circuit Test in order to check the correct PCB assembly. During this phase it is also downloaded the firmware relevant to the microcontroller managing the RF/Modem parts.
Functional Test: In this phase the single board is assembled onto the ODU baseplate and equipped with the PCB cover. During this stage, software trimming and calibrations and a functional test checking Modem and RF performance are carried out. In case of any test fail, the Automated Test Equipment ATE work station allows additional tunings.
ODU Final Test: In this phase the ODU is completely assembled (including the diplexer) and connected to a test reference IDU; then through the IDU/ODU cable connector the system firmware is downloaded. In this assembly configuration, the ODU is completely calibrated and final tested (including some BER measurements).
All the above mentioned test are performed at room temperature, a Stability Test, to verify the ODU over the full temperature range (-33°C to 55°C), is carried out at a sample rate determined by the current performance margins. In the beginning the Stability Test is performed with 100 % sample rate.
It is worth remarking that each test does not require any clean room environment being all the devices dies completely protected.

4. TEST RESULTS

At present, the status of the development is at pre-series stage just before mass production; all the specification targets were met with sufficient margin in accordance with ETSI Standard EN 302 217-2-2 and with the goal performance indicated in table 1. Fig. 9 shows a spectrum mask at RF level (38 GHz), and relevant specification mask, a BER performance is shown in Fig. 10; it is worth remarking that both specification are largely met. A following phase dedicated to collect statistical data and then determining production margins is under progress. Preliminary data are very encouraging and although some parameters margins had a slight decrease the overall technical solution is resulting very attractive.

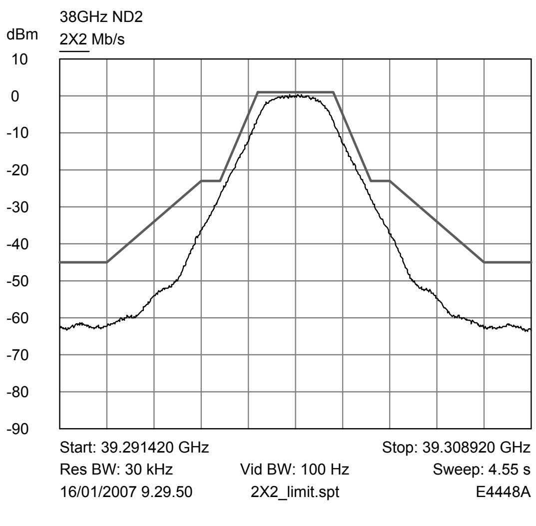

Fig. 9 -. 38 GHz Spectrum mask in 2x2 Mb/s configuration with specification mask.

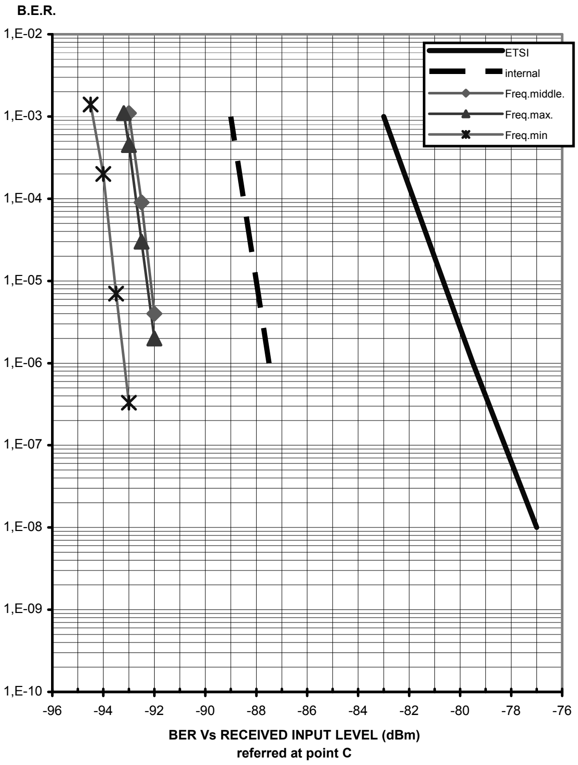

Fig. 10. 38 GHz BER performance in 2x2 Mb/s .

5. CONCLUSIONS

This PDH radio family derives from the evolution of a previous one in which Modem and MW Transceiver were allocated in two different sub-units; moreover in the higher frequency bands, the MW parts consisted of bare dies devices assembled with chip & wire technology in a clean room environment. Goal of the present development was a strong cost reduction both in term of devices/materials and manufacturing process without affecting RF performance. At present the development is at pre-series production stage, actual data, apart some margin decreasing about RF parameters, resulted to be fully compliant with ETSI Standard EN 302 217-2-2.With reference to the previous design we also obtained a 35 % cost saving and 30 % manufacturing time reduction.

6. AKNOWLEDGEMENTS

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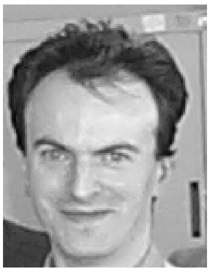
BIOGRAPHY

Marco Piloni received his “Laurea” degree in electronic engineering from the Politecnico of Milano in 1982. After serving in the Army, he joined in 1983 GTE Tel. as RF engineer for satellite equipment. In 1992 he joined the R&D department of Siemens Netwoks S.p.A. where at present manages a microwave laboratory for the development of ODU equipment: In the past he published several papers both in the European Microwave Conference and in the International Microwave Symposium; he is also author of some patents related to the microwave field.

Sergio Bianchi was born in Pavia, Italy in 1957. He received the “Laurea” degree in Electronic Engineering from “Università degli Studi di Pavia” in 1983. He joined Siemens Networks S.p.A. (formerly GTE Telecom) in 1984 and has engaged in research and development of radio modems. His research interests include modemodulation, digital signal processing and coding applied to digital radio links. He is author of papers and holds patents.



Giuseppe Montiron received the “Laurea Degree” degree in Electronic Engineering from the “Universita’ degli Studi di Pavia” in 1988. In 1989 he joined R&D optical fibers labs of Siemens TLC, now Siemens Networks S.p.A. in Cassina de’ Pecchi (Milan) as circuits designer for STM-4 equipment.. In 1993 he was involved in the design of the IF and control subunit for the Siemens Low Capacity Radio Links family (SRAL). He was also responsible for the ODU integration. He presently designs IF circuits and manages several project designs for ODU developments..