AN INDOOR UNIT WITH INTEGRATED ADM

A. Dal Lago, A. Eggenhöffner, R. Rezzonico

Siemens Networks S.p.A. - Cassina de' Pecchi (MI), Italy

Abstract: This paper describes the ADM version developed in the SDH SRA4 family. This split radio system, covering all traditional RF frequencies from 6GHz up to 38 GHz, allows an easy capacity management thanks to IDU modularity and flexibility: capacity ranges from 21xE1 to 2x(2xSTM-1) on a single carrier. The complete path from source to destination is protected either by radio switches or by SNCP. *Copyright © Siemens Networks S.p.A. 2007*

Keywords: Communication Systems, Digital Radios, Hardware, Integrated Circuits, Microprocessors, Performance Monitoring, Synchronization.

1 SYSTEM OVERVIEW

The increase in the demand for mixed voice and data transport solutions is a well known defying reality that is faced everyday from both operators and system suppliers. In order to match this need, the winning features of any new system can be considered to be efficient spectrum usage, flexible capacity and easy expandability.

In order to match these needs at best, the SRA4 SDH Radio family was developed in Siemens Networks S.p.A. labs in Italy. SRA4 is a split Radio system optimized for medium or high capacity radio links.

SRA4 covers all frequency bandwidths from 6 to 38 GHz for all standard channel arrangements (ITU-R and OIRT). Furthermore, the development of wideband ODUs allows a high flexibility degree, being the channel frequency selectable via SW and making also the ODU capable of managing customized channel arrangements.

Of course, whenever radio frequency is concerned efficient spectrum usage is also a well know 'must'. In SRA4 system this is guaranteed by dual polarization co-channel transmission, achieved with a fully digital cross polarization interference canceller, and by the capability of handling all modulation formats from 32 to 256 TCM. All this is obtained by means of simple software selections, and is the last but not least feature. The Reed Solomon plus Viterbi encoding ensures high performance improvement.

All these features allow agile system configuration and easy capacity management, ranging from 622 Mb/s (2x(2xSTM-1)), or to Gigabit Ethernet transport, or down to 21xE1 in the ADM built-in IDU appliance.

1.1 IDU structure.

The IDU (see Figure 1 and Figure 2) is mechanically compatible both with N3 and 19" racks. A compact mechanical solution and an appropriate division of functional blocks into physical units grant the System high flexibility, modularity and compactness.

Basic blocks are BB&Modem units, NE Controller and Alarm Unit.

BB&Modem units. IDU architecture allows equipping up to two BB&Modem units. BB&Modem units can be either 1x or 2xSTM-1&Modem type or ADM&Modem type. The development of other interfaces such as E3 or Gigabit Ethernet is already foreseen or under way.

A *patch panel*, connected to the ADM&Modem Unit, allows supporting the E1 lines with different physical interfaces such as 75 Ω micro-coaxial, 120 Ω RJ45 or sub-D connectors.

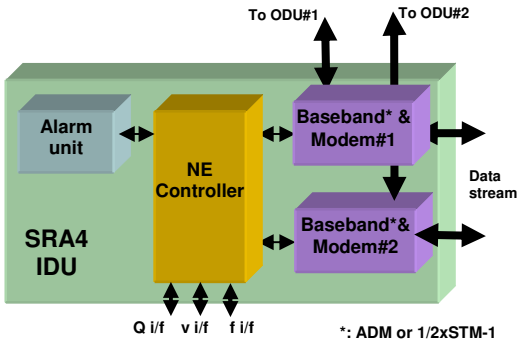

Figure 1 – IDU block diagram…

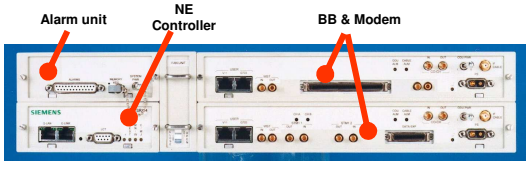

Figure 2 – …and real IDU.

NE Controller. It handles communication between Network Management System and Network Element: it collects and transmits to NMS alarms and measures from units, and activates commands coming from local or remote Supervision System. Furthermore, it manages the storage of System configurations on an E2PROM for automatic System restart. Of course, it grants also a connection towards a local PC (f interface) to completely configure and check the Equipment.

Via *Alarm Unit*, it makes possible to get summarized alarms on a public area connector.

A multilayer backplane gives the suitable wiring among the cards. All the user connectors are available from the front panel of IDU unit, thus allowing a fast installation and commissioning, and rack space optimization.

A single cable connects the indoor and the outdoor units.

1.2 System management

A user-friendly interface, LCT LinkViewer, was developed in order to meet installation requirements on a link basis, allowing easy system configuration (e.g. cross-connect set-up, see **Figure 3** and **Figure 4**), set-up and commissioning operations, and management of Security, Fault, Metering and overall system Performance as well.

SRA4 ADM built-in can be fully managed also by NetViewer, the Radio Network Manager developed for all Siemens Networks S.p.A. radio Systems, being also open to management by third party Management Systems.

1.3 Performance Monitoring

Complete Performance Monitoring is available, allowing a check of signal quality and a correlation to propagation conditions.

More in details, all the following parameters are available:

RSPI parameters, such as Received / Transmitted Level Tide Marks, Received / Transmitted Level Threshold Seconds, for each radio channel;

RPS parameters, in case of ADM built-in IDU only the Protection Switch Actual Count for (1+1) system configuration;

Quality parameters, related to each section and path termination: Errored Seconds, Severely Errored Seconds, Background Block Error;

Unavailability indicators also related to each section and path termination; Unavailability Seconds and Outage Intensity;

Pointer adjustment counters, related to any MST.

For any *plesiochronous physical interface,* Severely Errored Seconds, Unavailability Seconds and Outage Intensity information are available.

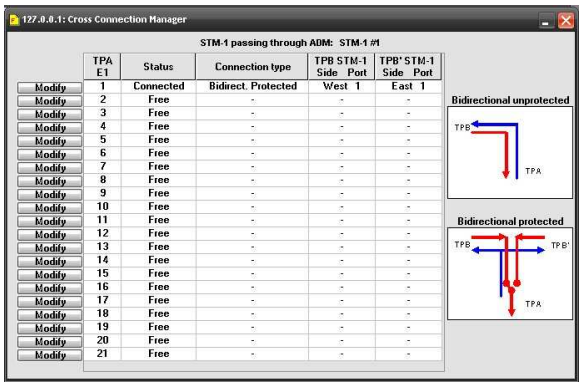

Figure 3 : Connection set-up.

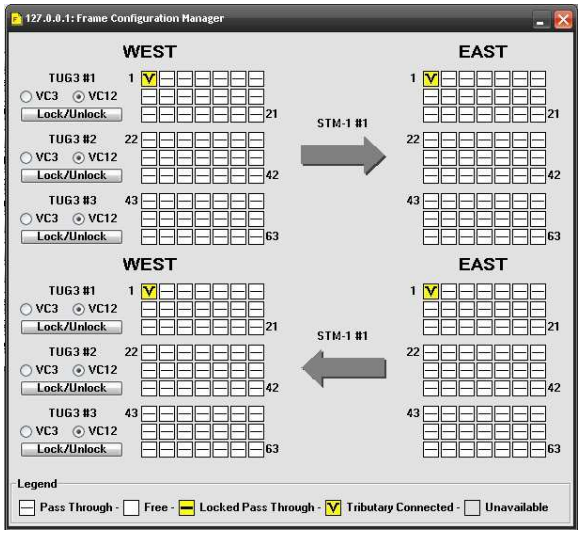

Figure 4 : Connection set-up.

1.4 Synchronization

As said before, ADM built-in IDU implements also MS termination: this means that it manages synchronization of all outgoing STM-1 signals according to ITU-T G.803 and G.813.

More in details, each ADM-1x/2xSTM-1 Board can select a proper synchronization source among an available set. The foreseen sync sources can be divided into internal and external sources. Internal sources are extracted from aggregate signal entering from each radio port. Available external clock inputs are a 2.048 MHz clock, and a possible clock extracted from one of the 21 E1 input tributary lines.

Proper synchronization source is selected on the basis of its quality level (either described by S1 byte content or by user setting) and of its priority level set by user.

S1 byte inserted in outgoing SDH frames is of course duly managed.

A synchronization output is also foreseen.

2 ADM&MODEM UNIT

2.1 ADM Board

The 1x or 2xSTM-1&Modem unit manages up to 2xSTM-1 interfaces (electrical or optical) and relevant RST processing, while present ADM&Modem unit manages up to 21 E1 data streams, with relevant RST, MST, High Order and Low Order Path Terminations, path protection and cross connection.

The simple block diagram shows the most important used devices and the most important logical connections.

There are a Line Interface Unit for the handling of the E1 physical channels, an ASSP device for ADM functionalities, a FPGA for SDH functionalities and two devices for the synchronization section.

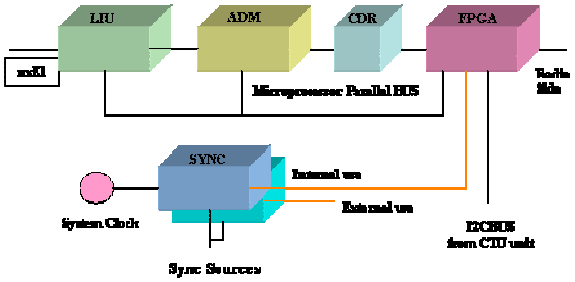

Figure 5 : ADM unit block diagram

Each E1 tributary signal is mapped in a VC-12 before being transmitted in an STM-1 signal. On the contrary, E1 signals are extracted (demapped) from VC-12 before being transmitted on the tributary lines. The ADM block is able to handle up to 63 VC-12 per each SDH port while the add drop capacity is up to 21 VC-12.

The board can be configured in three different connection types:

Unprotected bidirectional: a tributary line is connected toward only one of the two SDH ports.

Protected bidirectional: entering E1 signal is duplicated and transmitted towards both the SDH ports, whereas one of the two received SDH VC-12 shall be selected to be transmitted towards the tributary line. This mode suits well networks with ring topology.

Add drop: tributary signal is dropped from one of the SDH ports and the entering E1 is inserted to the opposite SDH port.

The STM-1 signal passing through the ADM block must contain three TUG-3s mapped in a VC-4 in order to be properly managed.

After the VC-4 has been divided into the three TUG-3, the ADM block shall be able to manage the following structures:

a TUG-3 containing a TU-3: the VC-3 contained in the TU-3 passes through the ADM block without any modification, only TU-3 pointer may be modified (see Figure 8, TUG-3#3).

a TUG-3 containing seven TUG-2: each TUG-2 may indifferently contain:

one TU-2: the VC-2 contained in the TU-2 passes unchanged through the ADM block, only TU-2 pointer may be modified (see Figure 8, TUG-3#2);

three TU-12, each one containing one VC-12 or a VC-11 "converted" in a VC-12, each VC-12 shall be separately transmitted towards the ADM (see Figure 5).

Of course, it is very important to realize VC2/VC3 passing through, because, even if this board does not perform add/drop of these virtual containers, other Network Elements belonging to the same network could manage them.

In Figure 6, Figure 7 and Figure 8 it is shown what above explained.

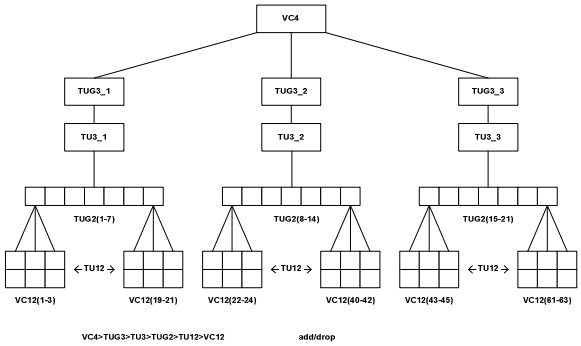

Figure 6 : ITU-T mapping example

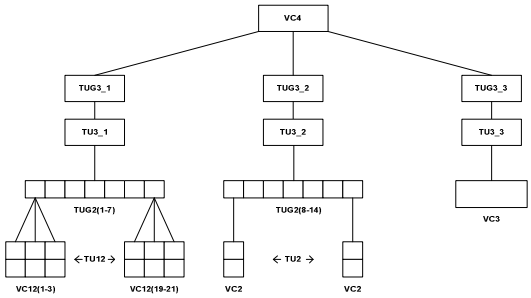

Figure 7 : ITU-T mapping example

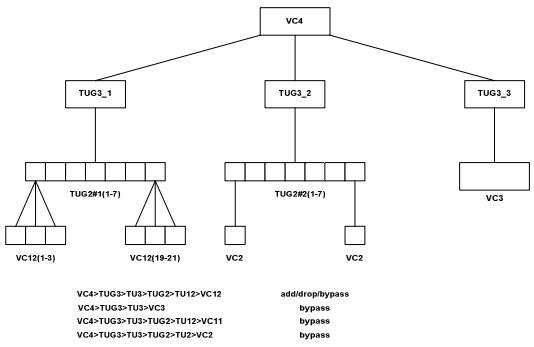

Figure 8 : ITU-T mapping example

The used ADM component is a highly integrated solution for compact transport systems working at

155Mbit/s radio interfaces. The feature rich device integrates a complete SONET/SDH subsystem including VT/TU/STS/AU memory based cross-connect capable of handling multiple network topologies, including 1+1.

The device supports both line and equipment redundancy. Two SONET/SDH network interfaces with 155M of both low-order and high-order pointer processing per-port are provided for line redundancy.

In order to realize protection functionality and some system configurations, each 1x/2xSTM-1 or ADM board exchanges the transmitted and received streams with the corresponding board in the contiguous slot (2x622 Mbit/s throughput via backplane). These data are carried serially; the parallel/serial and serial/parallel conversion is achieved inside the FPGA by particular macro (giving further advantage in terms of both space and cost reduction).

Each 1x/2xSTM-1 or ADM board receives from the neighbour Modem board information related to signal quality of this radio link. These are passed to the other board, so that each could determinate the best performance link (in order to properly activate switch protection). We have decided to transport these information through a proprietary frame. Comparing with the wire transport solution, the advantage is greater in the N+1 system.

A Way Side (2.048 Mbit/sec) and two auxiliary channels (64 kbit/s) are managed. These channels are exchanged between two RST and for this purpose the SDH bytes are used. For the 1x/2xSTM-1 board, which is foreseen in 'RST only' systems, we have implemented a proprietary mechanism in order to preserve the parity.

Information related to IDU-ODU connection are carried in a dedicate frame: commands to ODU, alarms from ODU and a 64 kbit/s channel for the IDU and ODU controller communication. In the 1x/2xSTM-1/ADM FPGA a proper modulation of this frame is realized.

Moreover there is an automatic power control mechanism to configure and manage all parameters related to control of the RF transmission power level, ATPC (Automatic Transmit Power control). In fact the ATPC strategy is managed by IDU software and firmware, while ODU provides to IDU the Prx values and carries out the ATPC commands decided by IDU. Using this strategy it is possible to control the power to handle a fading speed up to 100 dB/s.

The hitless switch is managed inside the FPGA. A dedicated logic is able to individuate the phase difference between the two received data streams and to balance the standby one in order to prepare the condition for such switch. Besides, it is communicated to NE Controller the phase difference between the two signals. A phase difference compensation of ±3 bytes was considered adequate.

In system with MST, even if it is not a recommendation requirement, it is possible (via presetting) that some MSOH bytes of the received frame are inserted in the transmitted one. Of course, if the transmitted frame is not synchronous with the received one, every now and then there could be a slip. Anyway, for the type of data and the slip frequency it is an accepted behaviour.

The density of the used components is very high (see Figure 10, which for sure does not give it evidence enough).

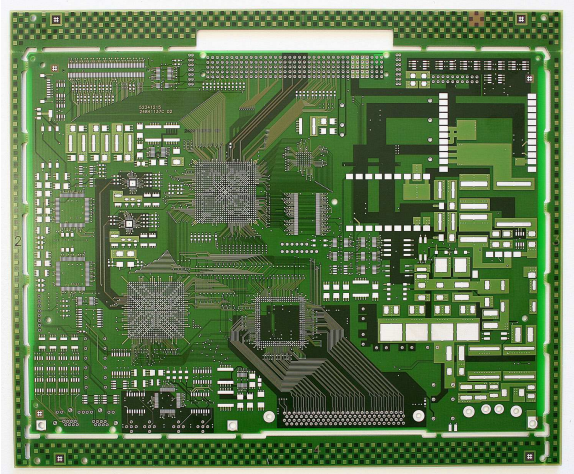

Figure 9 : Board photo w/o components …

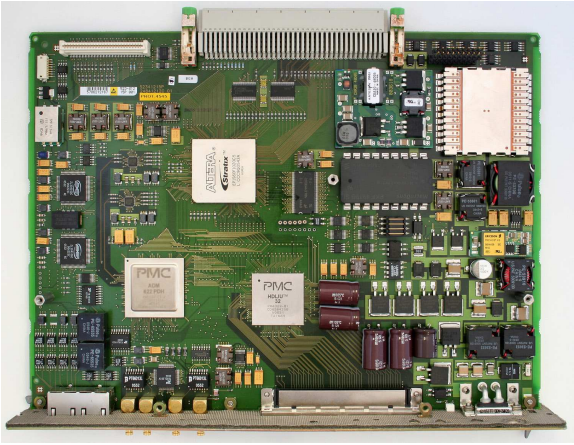

Figure 10 : ... and with components.

It was necessary to develop the board layout using high technology (blinded laser drills) due to Ball Grid Array component presence and to a high number of layers (12). Moreover there are some critical parts in term of frequency and then it was necessary to take of the integrity of these signals. In fact there are some connections working up to 155 MHz. Some of these are internal connections between the chips; others are towards the contiguous board. There is also a 46 wire connection between the FPGA and a Synchronous DRAM working at 60 MHz.

It is important to highlight the high number of connections in order to link the different chips.

Other connections work at no such high frequency (up to 40 MHz) but required high number of wires and then it was necessary a very careful layout study in order to avoid noise, disturb and cross-talk problems.

Board dimension 20x27 cm		
12 layers		
643 components		
Nets about 5400		
Blinded laser drills ϕ 0.2mm layer 01		02
Blinded laser drills ϕ 0.2mm layer 01		03
896 pins	FCBGA 31x31 mm	
276 pins	L2BGA 27x27 mm	
1020 pins	FBGA	
Environmental Conditions:		
stationary use -5 +55°C		
Power dissipation 15 watts		

Table 1 : Highlights

2.2 Embedded Microprocessor Acting

As previously said, the NE Controller collects alarms and measures from Units and activates commands from Supervision System: all that is realized by write/read operations through a System Bus.

In the IDU, the system bus connects all the devices (which must receive or give information) of all the Units.

The System Bus is the Philips' I2C-Bus (Inter-IC ©) and the components we used carry of course the I2C logo by Philips. This well known, low cost bus (designed by Philips several years ago) with only two bidirectional lines allows a communication link between several devices.

Every 1x/2xSTM-1-Modem Unit can be indifferently inserted in the upper or lower slot (see Figure 1). The Unit grasps its position by means of a proper key on the backplane: so it can correctly hold the bus only when addressed (avoiding conflicts).

The FPGA devices are programmed by the NE Controller, which stores the programming data in a flash memory (for cost, space and power consumption optimization).

Every Unit has an I2C-Bus I/O Expander device where the Unit Type and the FPGA identifier are wired: so the NE Controller (before programming the FPGA) can acknowledge these information asking the I/O Expander through the System Bus and programming the FPGA with the opportune data.

When an ADM Board parameter is changed by the NE Controller, the input arrives to the ADM FPGA always through the System Bus (see Figure 11).

If the information are relevant to the FPGA, they are processed by the same FPGA with glue logic and they are written into the FPGA Registers. On the contrary, if the information are relevant to other devices, they are processed by the FPGA embedded microprocessor (NE Controller Interface). The embedded microprocessor translates and stores these information into an elastic store (inside the FPGA).

The embedded microprocessor reads from the elastic store and executes the command writing into the involved devices (ASSP Interface). After any command execution, the embedded microprocessor reads and executes another one command if present.

The elastic store is necessary because a single write operation of the NE Controller can lead to many write operations on both the commercial devices. So many other commands could arrive before the embedded microprocessor has executed all of them.

The elastic store dimension was calculated in order that, even if the NE Controller continuously wrote in it at its maximum speed, the buffer would not fill, because the FPGA write operations are faster than NE Controller ones (through the System Bus). Anyway, for safety reasons, if the elastic store filled more than a reasonable threshold, the FPGA would not give any more the acknowledge to the write/read System Bus operations (stopping NE Controller) till the buffer is empty.

All that is pretty similar to the method described in the Unites States Patent 4171538.

The ADM FPGA embedded microprocessor continuously reads the commercial device registers. It collects the data for the NE Controller, realizes a first integration and writes them into the FPGA registers. So the NE Controller can read them more slowly without obstructing the System Bus with not much significant data and without data loss.

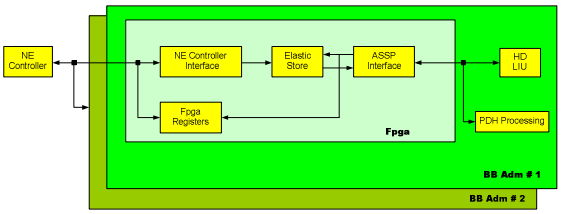

Figure 11 : Embedded microprocessor acting.

The embedded microprocessor can be considered acting as a slave of NE Controller. Moreover, it executes some advanced procedures such as SNCP: it reads some external registers and in conformity with the signal quality (local alarms such as AIS, Loss of Pointer, Unequipped, PLM and TIM), eventually writes the commercial device registers, realizing the SNCP protection of 21 VC12. Switching is independent for each tributary line. The protection is not revertive, and it is performed within 50 ms.

As far as synchronization is concerned (see paragraph 1.4), the user chooses two couples between the aforementioned sources: Internal Synchronization Source A/B (ISS source A/B) and External Synchronization source A/B (ESS source A/B). The NE Controller imparts them to the FPGA (see Figure

12). The embedded microprocessor selects the internal source choosing it between the two ISS sources. It chooses the highest quality one, or (if they have the same quality) the highest priority one. If both are alarmed the holdover status is forced.

In analogue way, the embedded microprocessor identifies the external source. This source is available as a 2048 kHz synchronization interface (T12), according to ITU-T G.703

When a failed source returns in working conditions, a "wait to restore time" shall pass before the embedded microprocessor shall consider it available again.

The 'free-running' status is either forced by user, or set at system start up or set when holdover mode is no more available.

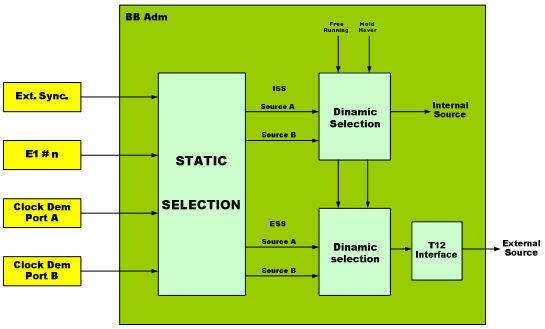

Figure 12 : Synchronism selection.

2.3 Modem Board

The modem is based on the SCM chip, described in a previous ECRR [1], and has an optimized analog design. Together with the aforementioned FPGA, its flexibility allows the SW configurability of system that is the transport of an STM1 stream in channels spaced 27.5, 28, 29, 29.65, 30, 40, 50, 55 or 56 MHz and a capacity of 2xSTM1 in channels spaced 50, 55 or 60 MHz. With co-channel operation two modems, sharing the same frequency band, can double the capacity and the spectrum efficiency with the possibility to reach the STM4 capacity.

The modulation scheme ranges from 32QAM to 256QAM. The error correction is concatenated Trellis Code Modulation (TCM) and Reed Solomon. The Trellis Code Modulation (TCM) codec can be two or four dimensional, the Reed Solomon can correct up to eight byte errors in a block up to 255 bytes long.

This extreme flexibility can be reached only with fully digital clock and carrier recovery loops, so we have no dependency from the symbol frequency and we can choose the coding scheme that is optimum for the radio system that we want to assemble. An interleaver separates the concatenated codes and another one protects the pointers of the SDH frame and the header of ATM cells if transported.

In receive side the analog parts are reduced to an automatic gain control (AGC) circuit and some filtering, because direct intermediate frequency sampling is used for the main path and the cross polar interference canceller (XPIC) path.

The demodulation is digital with a Hilbert filter and automatic frequency control (AFC). The carrier recovery loop is after the adaptive time domain equalizer to minimize the delay inside the loop. In this way it is possible to have a wide bandwidth to cope with radio frequency local oscillators phase noise and frequency jumps.

The modem unit is designed to operate in a split system with microwave parts in the outdoor unit near the antenna. A single cable connects the modem and the outdoor unit; so transmit and receive intermediate frequencies are different. The same cable carries the aforementioned bi-directional supervision channel and outdoor unit power supply.

3 HIGH LEVEL SYSTEM FEATURES

3.1 Protections.

Propagation phenomena can heavily affect the received signal quality and a Radio System has to cope with this problem. In order to protect traffic against any possible anomalous condition and to match availability targets, a bunch of solutions are usually adopted, such as Hitless Switching and Hardware redundancy. These functions are an essential part of a Radio Terminal Equipment.

SRA4 IDU is optimized to equip a 1+1 configuration with hardware protection for any kind of interfaces. Moreover, a Frequency Diversity hitless protection is also possible, as well as the Hot Standby 1+1 protection. Easy expansion from standard 1+1 protected configuration towards multi-channel N+1 ($N \leq 3$) configuration is also possible by adding an Expansion IDU.

In the ADM configuration, SNCP protection is foreseen.

3.2 Possible system configurations

The main system configurations that are foreseen with ADM built-in IDU are summarized in Table 2.

System configuration	Capacity	On air
(2+0) with nxADM	up to 42 E1	STM-1, 2xSTM-1
(2+0) with protected ADM	up to 21 E1	STM-1, 2xSTM-1
(1+1) with ADM	up to 21 E1	STM-1, 2xSTM-1
2x(2+0) Co-Channel with ADM	up to 42 E1	STM-1, 2xSTM-1

Table 2- Main system configurations.

(2+0) with nxADM. This can be considered the basic system configuration. Two 1x/2xSTM-1&Modem cards are equipped in the IDU, one being of course of the ADM&Modem kind. In Figure 13 the configuration with two independent ADM/Modem cards in the IDU is shown: this allows adding/dropping up to 42 E1 tributary signals from the same STM-1 signal or up to 21 E1 tributary from each one of the two STM-1 data stream.

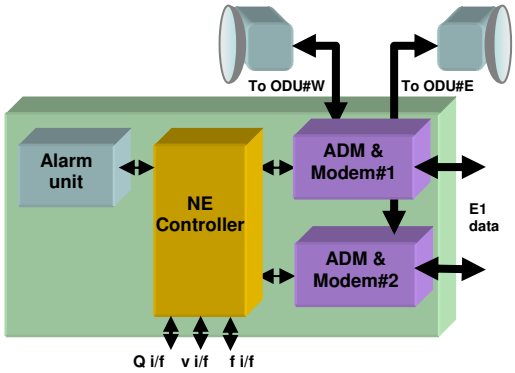

Figure 13 – (2+0) with 2xADM.

(2+0) with protected ADM. In the case of Figure 14 add/drop action is carried on 21xE1 on one of the two STM-1 signals. The two ADM&Modem sub-units are connected to the same patch panel supporting the wiring for the protection functionality.

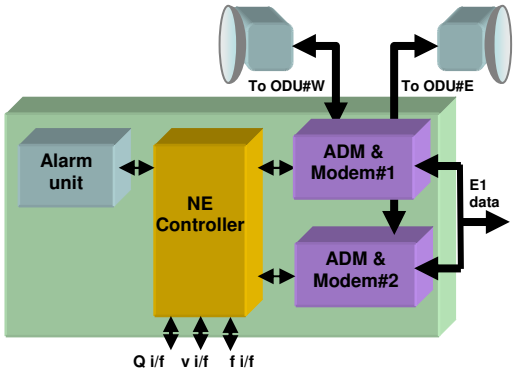

Figure 14 – (2+0) with protected ADM.

(1+1) with ADM. Figure 15 depicts the system layout when radio protection is foreseen. Radio capacity may be either STM-1 or 2xSTM-1.

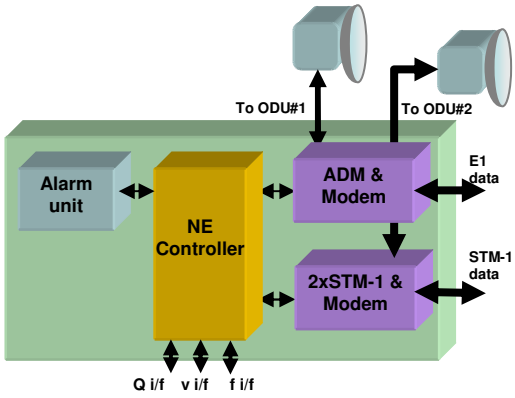

Figure 15 – (1+1) with ADM.

2x (2+0) Co-Channel with nxADM. Two independent radio signals for each direction are managed, sharing the same frequency with different polarization as can be seen in Figure 16. Network Element is formed up by two IDUs: "main" IDU contains the NE controller and one or two ADM&Modem cards, while the "expansion" IDU contains 2xSTM-1&Modem cards.

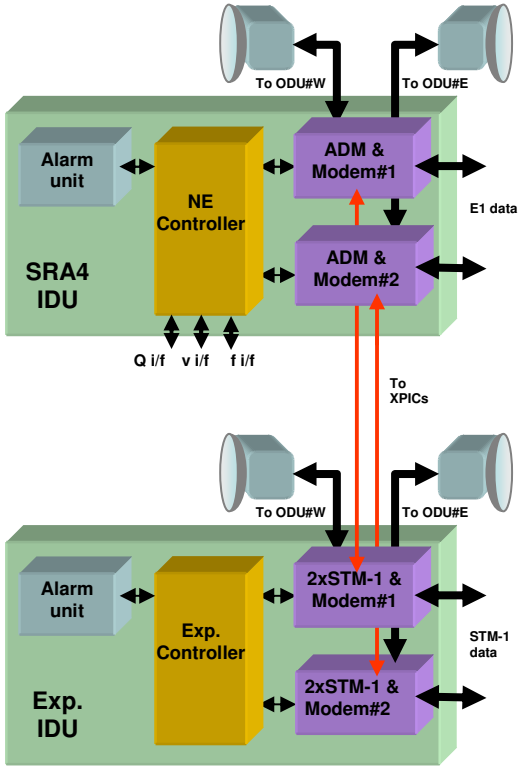

Figure 16 – 2x (2+0) CC with 2xADM.

4 CONCLUSION

The new ADM built-in IDU developed for SDH Point-to-Point split SRA4 System has been described.

The IDU is based on a compact architecture and has high flexibility, and compactness, thanks to a suitable modularity in functional blocks in the IDU.

The use of ASSP devices for the ADM functionality was done to optimize the time to market while the use of an embedded CPU processor inside the FPGA against an external device was done for a cost optimization, and for the high density component of the board.

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United States Patent 4171538: Elastic store slip circuit apparatus for preventing read and write operations interference

BIOGRAPHY

Antonella Dal Lago was born in Vicenza, Italy. She received the Doctor degree in Electronic Engineering from Politecnico di Milano (Milan, Italy), in 1988. In the same year she joined R&D Microwave Labs at Siemens Networks S.p.A (formerly Siemens Telecomunicazioni S.p.A), Cassina de' Pecchi (Milan, Italy). Since 1992 she was involved in R&D activities for Radio Systems as System Engineer, starting with High Capacity Digital Radio Systems and becoming in 2002 responsible for System specification and integration activities for SDH point to point radio systems. She is currently responsible for specification activities in point to point radio systems in Microwave Business Unit.

Andrea Eggenhöffner was born in Genova, Italy, on July 10, 1958. He received the Doctor degree in Electronic Engineering from University of Genova in 1985. In the same year he joined R&D Labs at Olivetti. In 1988, he joined the R&D Transmission Laboratories at Siemens Networks S.p.A. (formerly Siemens Telecomunicazioni S.p.A.), where he was involved in activities related to digital processing signals in SDH Optical and Radio System developments. Since 2000, his research interests include PDH Radio System developments, too. He is presently responsible for a Base Band laboratory in the Microwave Business Unit.

Roberto Rezzonico was born in Milano, Italy, on April 16, 1963. He received the Electronic Engineering Doctor degree in 1988 from Politecnico University in Milano. In 1990, he joined the R&D Transmission Laboratories at Siemens Telecomunicazioni S.p.A., presently Siemens Networks S.p.A., where he was involved in activities related to digital processing signals in SDH and PDH Optical and Radio Systems developments. He is currently responsible for a Base Band laboratory in the Microwave Business Unit.