ARCHITECTURAL SOLUTIONS AND IMPLEMENTATION FOR A WIMAX BASE STATION

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Abstract: The purpose of this paper is to present the architecture and the practical realisation of the Base Station compliant with 802.16d IEEE standard developed for the WayMax@Advantage® system. This system, including the terminal station (CPE), has been developed by Siemens Networks laboratories.
A brief system architecture overview is presented, followed by the description of the main units componsing the BS: the OutDoor Unit, the MAC-DLC and the Modem.. Unit architecture and functionalities, HW and SW implementation main aspects are here presented.

Keywords: Waymax, ODU, MAC-DLC, modem

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1. INTRODUCTION

The design of a compact Base Station compliant with IEEE 802.16d standard is a very challenging task. WiMAX system actually requires high performance RF parts, suitable to provide high output power and very low sensitivity threshold, and powerful digital blocks, for physical and MAC layer processing together with IP packet handling. This paper describes the base station developed by Siemens laboratories. The system architecture is as shown in the figure. A single indoor rack houses up to five SMU units (Sector Controller Modem Unit). The rack contains also two redundant Controllers and Switch Unit (CSU) as well as the Connector/ Unit. Each SMU is connected to the relevant ODU unit (typically one ODU per sector).

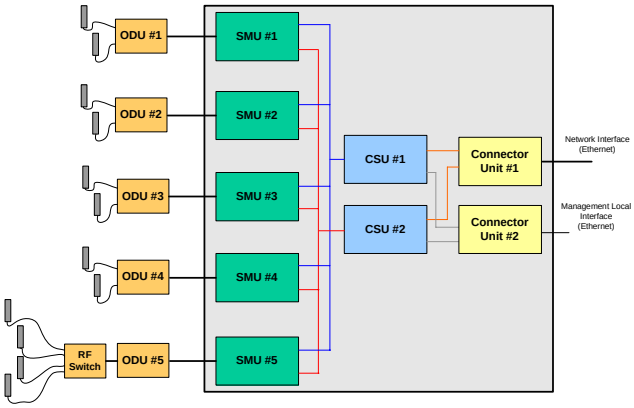


Fig. 1. Base Station Architecture

2. OUTDOOR UNIT

2.1 Architectural Description

The Outdoor unit has been designed in order to provide the suitable RF Output Power and "manage" the received signal for both main and diversity path. The ODU block diagram is shown in fig. 2 and fig. 3 for the TDD and FDD solution respectively. First it is very important to underline that the same structure is suitable for TDD application and FDD application as well: in fact exploiting this kind of structure the TDD solution can be achieved just setting the frequency shifter to zero, that is to say it is possible to carry out the "TDD mode" starting from the "FDD mode" simply by a SW setting. The result is a very simple and flexible architecture. As the ODU works in "TDD mode", the needed isolation between TX and RX is achieved by using an isolator instead of the diplexer filter (see fig. 2 and fig. 3), of course, the switches are controlled in such a way to avoid TX/RX overlapping. The RX IF (both for the Main and the Diversity receiver), the TX IF, the reference frequency used to lock the ODU PLL, as well as the FSK link between ODU and IDU run at the same time along the IDU–ODU cable connection. (This cable is, moreover, used to provide the DC bias to the ODU).

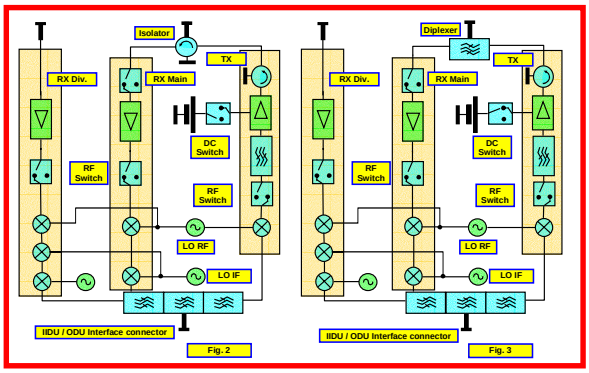


Fig. 2 TDD ODU Block Diagram
Fig. 3 FDD ODU Block Diagram

2.2 ODU Electrical Characteristics

The TDD ODU Way-Max solution works at 2.4 GHz (more precisely 2.3-2.5 GHz). As far as the FDD solution is concerned, the design has been developed for the 3.4-3.6 GHz frequency band. The main problem has been found in designing the power amplifier. In fact a significant work has been made in agreement with the power component supplier (Infineon and Freescale) to carry out the suitable performance to meet the WiMax standard specs: in practice a new generation of Low-Cost LD-MOS device has been introduced. The same technology has been used for both 2 and 3 GHz application. The result looks very good: a 37 dBm output power amplifier has been achieved reaching considerable performance from both linearity and efficiency point of view (more than 12% efficiency for the whole line-up). As far as t the linearity is concerned (EVM) the results are shown in fig. 5 and fig. 6 (3GHz and 2GHz solution respectively).

2.3 ODU Practical Realization

The ODU has been realized, mainly, by using two PCBs: the first one concerning the Receiver (Rx main and RX diversity). This board include the bias system the IF section and digital TX and RX management. The PCB board is a simple FR4 RoHS compliant. The second PCB is concerning the Power Amplifier: “Rogers” substrate has been used in order to face problems owing to the losses, and substrate electrical parameter spreading as well (see fig. 4). The ODU on the whole is depicted in fig. 7

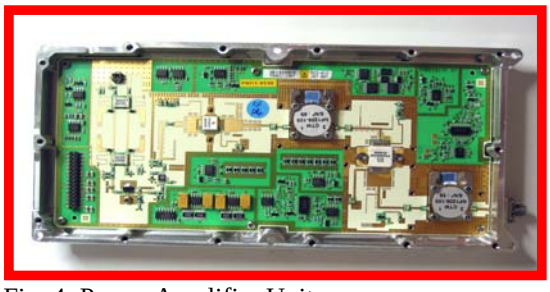
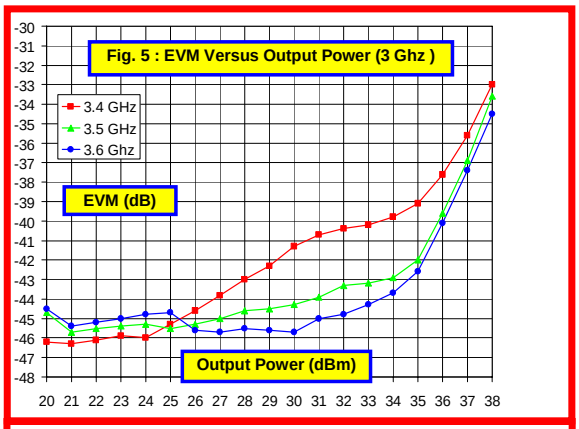
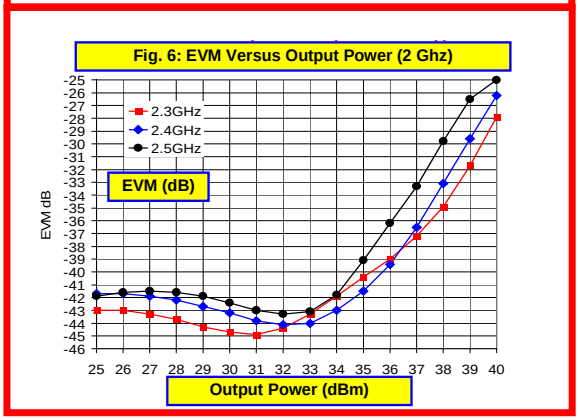


Fig. 4: Power Amplifier Unit





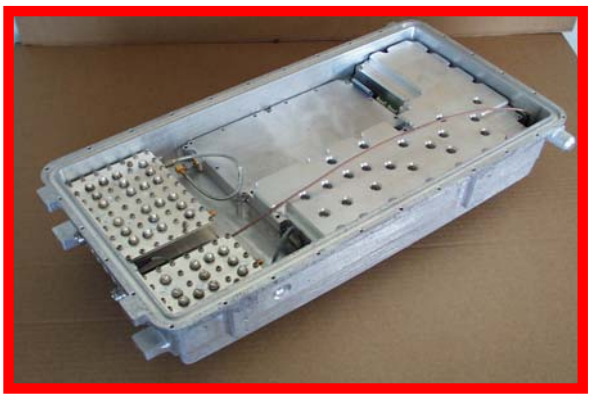


Fig. 7: OutDoor Unit Inside View

3. MAC-DLC UNIT

3.1 General Description

The MAC-DLC implements all the MAC and Switching functionalities according to 802.16d WiMax specification and with the Modem sub-unit forms the Sector Modem Unit (SMU) of WayMax@Advantage® BS. The MAC-DLC can be mainly divided in the following macro blocks: Data processor, Control/Mgt processor, Communication interfaces, System memory and Base functions.

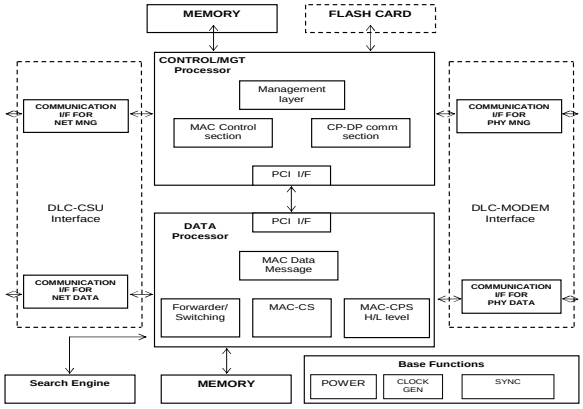


Fig. 8. MAC-DLC Block Diagram

3.2 Data Processor

This processor manages the data traffic from/to Network side to/from Radio side implementing MAC Data layer and Packet Switching functions. The main SW modules supported on data processor are briefly reported in the following.

MAC-CPS Low-Level (RISC-implemented): performs heavy computing and repetitive functions like MAC-PDU/SDU building, encryption/decryption feature, packet header parsing and checks the correctness of the MAC-PDU (CRC-32 for payload, HCS for header). RISC microcode with Security engine are used to offload the SW runs in the core processing. In DL direction (PDU Builder), all SDU received from Network side are reduced to fragments and/or packets enveloped in PDU sent to the Modem. In UL direction (SDU Builder) all fragment and/or packets received from Modem are re-assembled to complete SDU.

MAC-CPS High-Level (CORE-implemented): performs all advanced and highly flexible features regarding traffic scheduling, map messages, fragmentation/packing, initial ranging and phy/power adaptation. These processes are software implemented on core processor with optimized tasks run with data/instruction caching mode to obtain a high performance in terms of data throughput and stability, in the following a brief description of the main functions are summarized. UL /DL Scheduler is a main task that decides, frame-by-frame, the UL frame access, processing the bandwidth requests from all the terminal stations registered in the sector and the composition of DL frame on the base of the local packet queue status. MAP Builder manages all the standard MAC Map Messages (DLFP, DL-MAP, UL-MAP, UCD, DCD) to inform terminal stations and proprietary messages to inform Modem about frame structure.

Fragmentation, Packing, Concatenation are additional MAC-Data functions available in UL/DL scheduling MAC PDU to allow efficient use of available bandwidth for QoS requirements.

Initial Ranging is the process for the correct timing offset and power adjustments to reach the alignment of the terminal station to the base station. This process of equalization in time and power is the first phase of network entry procedure completed with MAC control layer. PHY and Power Management mode is the process to adapt the physical profile (power and modulation type) of each terminal station to the radio link condition. In UL the procedure controls the values of CINR and BER in a polling cycle to determine the correct physical profile. In DL the terminal station may ask to change at a physical profile through a DBPC messages. The requests profile will be accepted in order of rules fixed in the LCT tools.

MAC-CS (CORE-implemented): adapts upper layer protocol data to 802.16d MAC structure and manages all features regarding traffic classification for QoS functionality. Packet Classification, actually based on TOS or VLAN parameters, classifies and maps the DL traffic according to classification rules defined CID by CID. PHS operation (Header compression) consists in compacting the header of input SDUs to skip items not to be transmitted.

Forwarder/Switching: forwards the downlink packet data to the destination MAC address in the same way as level-2 switch searching for the associated outgoing port (terminal station). Every time an uplink SDU is received, the source MAC address is examined and is looked for in the forwarding table via search engine. If it is already present, its ageing time is up-dated; on the contrary the MAC address is learned and inserted in the forwarding table. All the basic functionalities of switching are supported: auto learning, flooding, filtering, forwarding table and ageing time. Two forwarding modes are supported: in unprotected ports packets received from any port of the forwarder can be redirect towards any other port, while in protected ports the direct communication between distinct ports of the switch is not allowed; packet should be forwarded only to network port.

3.3 Control Processor

This processor manages all the control plane messages and procedures with the terminal stations according to 802.16d WiMax standard specifications, also controls and activates the configuration requested from system management layer to MAC data/control planes. MAC Control section mainly performs the standard procedures for network entry and traffic connection setup/delete, the main functions are summarized below. The TS registration procedure starts the associated state machine as soon as data processor notifies the end of ranging phase to complete the network entry with management CID assignment. The Service Flow (SF) procedure provides the activation of traffic connection provisioned by management layer as soon as TS network entry is completed, these operations are managed via standard messages (DSX procedures). The Type-Length-Value (TLV) procedure executes the formatting scheme that manages each

transmitted/received parameters inside the various MAC messages. The Security management procedure controls the TS authentication phase using different level of certificate and the generation of AK-key to enable the starting of the cryptographic process.
CP-DP comm section is involved in control of MAC data and control processor with commands, alarms, and status to and from the system management layer. Dedicated communication channel on PCI interface is provided to setup data plane functions and to monitor activity via keep-alive procedure. System management layer controls all the MAC-DLC functionalities through an SNMP Agent that manages all MIB information exchanged with centralized network element card (SNMP Manager), in addition controls the outdoor radio part (ODU) through a TNMP Manager that manages the ODU MIB.

3.4 Communication Interfaces

On network side the communication interfaces connect the MAC-DLC card to Control/Switching unit (CSU), while on radio side with the Modem unit both for data and management information. I/F for phy--mngt implements all the functions to program and configure Modem FPGA and DSP while I/F for phy- data implements all the functions to transfer MAC data/control messages with Modem and Terminal Stations. I/F for net-data implements all the functions to transfer data packets with network interface while I/F for net-mngt implements all the functions to transfer management information between the network element manager and MAC-DLC. PCI interface is a communication channel between data processor and control processor, provides a dedicated messages protocol and a shared memory bank where each processor can read and write data.

3.5 System Memory

Both data and control/mgt processors have a set of memory for storing code and data, each processor has a Flash memory of 16 MB used for boot, eeprom emulation and code storing, and a Ram memory available in a bank of two SDRAM-banks, each of 64 MB.

3.6 Base Functions

The base functions concern different parts: power supply needs to feed the MAC-DLC, clock generator synchronizes the internal processes, the synch information incoming from CSU is forwarded to modem via SMU.
MAC-DLC is powered by two battery voltage with -48V, feeds also the modem subunit is fed via MAC-DLC subunit. By PLL are generated two different clock signals to synchronize the main process and to drive all communication stages like switch Ethernet and the FPGA-Search Engine. MAC-DLC receive an external synchronize of 10MHz and an impulse of 1Hz from CSU that will be switched to the modem.
Flash Card: provided only for stand-alone solution.

4. MODEM UNIT

4.1 Modem Architecture

A very flexible modem unit configurable for different canalization bandwidth has been design to manage all the signals concerning a sector, i.e. downlink stream and both main and diversity uplink signals. Due to cable interface used in the split architecture, based on IF signals, part of the analog processing as well as the digital one have to be implemented on the modem board. A high integration and a digital approach to the most functions has made possible to design a flexible system. The most mo-demodulation functionalities, implemented by means of digital devices and a very compact analog design have made possible a single board implementation necessary to have a compact SMU and then housing up to four sectors, plus redundancy, in a single rack.

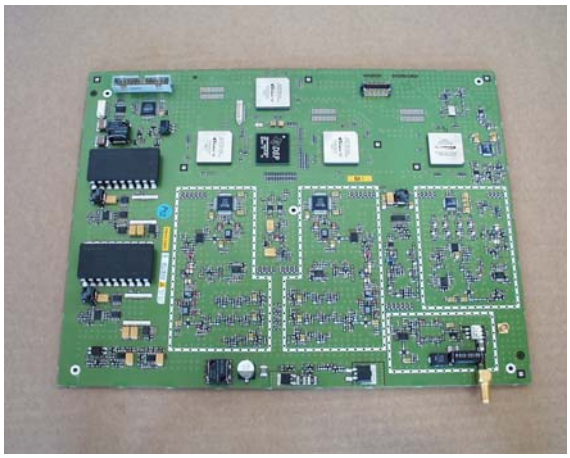


Fig. 9: Modem Unit

Modem architecture can be divided into three main parts: analog processing, digital processing and cable interface (IDU_ODU interface).

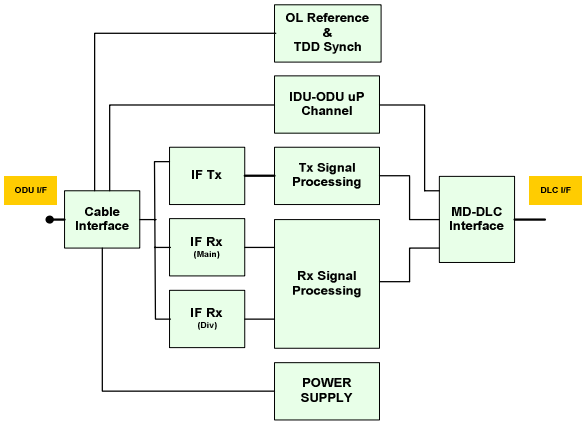


Fig. 10: Modem Block Diagram

4.2 Modem Analog Signal Processing

The required programmability and the specifications, highly demanding in terms of receiving selectivity, sensitivity, input dynamic range and transmission signal quality, i.e. EVM, set a very challenging task for analog blocks development. To obtain the needed selectivity and interference channel rejection for all the possible bandwidth, ranging from 1.75 to 14 MHz, the received signal goes through a group of switchable filters before been converted to digital domain where further digital filters are present. The huge dynamic of input signal level, more than 70 dB, is adjusted by digital attenuators changing their attenuation value on a burst by burst basis according to the foreseen level, making possible to reduce the number of bits of the analog to digital converter. On downlink side, the modulator is based on IQ baseband architecture. A trimming digital block reduces modulator inaccuracies, e.g. quadrature error, to get the required transmission quality.

4.3 Modem Digital Signal Processing

The digital blocks perform both symbol processing indicated by 802.16d WiMAX specifications and proprietary functionalities as diversity receiver signal combining, clocks generation and other function related to the implementation. A mixed architecture based on FPGAs and DSP devices has been chosen to achieve the required processing capacity and flexibility. Time domain processing as shaping, digital predistortion, filtering, etc., has been developed using FPGAs as well as the symbol synchronization block, including preamble correlation, delay estimation (ranging), both for traffic and ranging burst, and received input level estimation. The same devices have been used to implement the frequency domain processing, i.e. FFT, CP insertion and removal, preamble and pilot sequence generation, etc. User domain processing requires a most flexible approach as different operation have to be performed depending on the physical mode selected for each user. Mixed software-hardware architecture has then been designed, including digital signal processing device, FPGA and soft-micro. Channel estimation, equalization and diversity combining, as well as all tracking algorithm are carried out by the DSP, which send equalized data to the FPGA, where the microprocessor performs all the decoding operations exploiting hardware implemented blocks (e.g. the RS decoder). The digital part includes also clock generation, synchronization and frame management. In OFDM system symbol clock is strictly related to the bandwidth; then the possibility to select different bandwidth implies a clocks generation structure based on an NCO and including several PLLs to have the correct clock frequency for each configuration. Different frame lengths and cyclic prefixes, CP, are also selectable, requiring a programmable frame generation and synchronization block. Finally a high-speed interface, based on GMII standard, has been developed to interface the modem and the MAC-DLC boards, carrying data and information packets required to dynamically configure the radio interface.

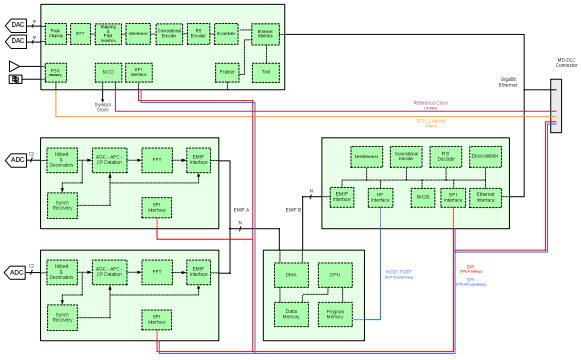


Fig. 11: Digital Signal Processing Block

4.4 Cable Interface

Connection to the outdoor unit requires power supply feeding, IF signals filtering, RF local oscillator reference signal and TDD synchronism transmission, together with a communication channel connecting the IDU microprocessor to the ODU one. Different signals, from DC to several MHz, are then multiplexed in the cable interface block by means of several filters. To guarantee compliance with Tx EVM requirements, a very low noise reference signal must be supplied to the RF oscillators. A critical circuit has been developed to generate an IF reference signal from the 10 MHz master clock without increasing phase noise.

5. CONCLUSIONS

A new WiMax System, compliant with IEEE 802.16d standard, has been introduced. The system has been described from the architectural point of view and some experimental results shown. The new system is suitable for both FDD and TDD application. More detail and design aspect will be presented in the paper.

REFERENCES

IEEE Std 802.16 – 2005 "Air Interface for Fixed Broadband Wireless Access System"

BIOGRAPHY

Luigi Antonio Cervi, received his electronic engineering degree from "Politecnico di Milano" in 1989. Then he joined Siemens TLC as an hardware designer in point to point MW systems: In particular concerning the OutDoorUnit . Since 1999 he is in charge of the MicroWave Laboratory of Siemens MW Department. He worked and designed on various ODU unit (PDH, SDH, Way-Max)

Alessandro Greco, received his electronic engineering degree from "Politecnico di Milano" in 1990, with a thesis on "Phase Fluctation of a Synchronous Network Output Signal", realized in Telettra S.p.A. In 1992 he joined Siemens TLC as an hardware designer in Radio Mobile Department. In 1995 he moved to the Medium Capacity Modem Laboratory of Radio Mobile Department where was involved in QAM modem development. Since 1998 he is in charge of the Poit to Multipoint Modem Laboratory of Siemens Microwave Department. He worked and designed on various Mo-demodulation projects of Radio System.

Angelo Pasotti, received his electronic engineering degree from "Politecnico di Milano" in 1982 with a thesis based on a SW program for "Automatic management of a medium size airport". In 1984 he joined the Switching Laboratory of ex-GTE in Milano as a designer in R&D Department. In 1997 he moved to System Engineering of Microwave R&D Department (Siemens TLC) where was involved in architecture definition of ATM Broadband PMP System. Since 1999 he is in charge of the Microwave Software Department of Siemens ICM where later is involved in architecture definition and system development of the WiMax Base Station.