Improving the dielectric losses of $(Ba,Sr)TiO_3$ thin films using a SiO_2 buffer layer

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Ferroelectric thin films are good candidates for the processing of agile devices like filters, phase shifters and antennas. This is because their high dielectric susceptibility can easily be tuned by a dc electric bias. The most studied thin films for this purpose are within the solid solution $BaTiO_3$-$SrTiO_3$ and the optimal composition is the so called 60/40 one ($Ba_{0.6}Sr_{0.4}TiO_3$ - BST_6 in the following). Even before thinking to any integrated device, there are several drawbacks raised by these BST_6 films themselves. The most difficult issue to overcome is linked to the intrinsic dielectric losses in BST_6 films. These dielectric losses are usually above 1% (i.e. above the threshold as set by the electronic industry) and increase when reaching the targeted frequency range (f>1GHz).

In ceramics, the composite route has been used from the beginning of the nineties to overcome such drawback. The idea was to add to the ferroelectric BST_6 grains a dielectric phase with very low dielectric losses. Such dielectric barrier in the high frequency range were selected within the already existing materials: MgO, $MgTiO_3$,… Starting with the same idea as for bulk ceramics, multilayers of BST_6 alternated with MgO dielectric barrier have been grown. However, the direct influence of this stacking on the dielectric parameters has not been quantified up to now. Our work follows the trend which has been initiated in our laboratory recently on using Silicon Oxide as a coating agent of BST_6 individual grains. Using radio-frequency magnetron sputtering, we transfered this Core-Shell concept to the integrated devices with a stacking of SiO_2/BST_6 layers, the main scope being to decrease the BST_6 losses thanks to the SiO_2 dielectric barrier. Doing so, we were able to repetitively achieve dielectric losses of 0.1% while keeping a high dielectric susceptibility and a suitable tunability.