Evolution of low sigma grain boundaries in PTC thermistors during sintering

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Abstract

BaTiO3-based PTC thermistors undergo a large and rapid increase in resistance just above the Curie temperature, Tc. The resistance increase is predominantly associated with an increase in grain boundary barrier height, although there is ample evidence for variations in the magnitude and form of PTC behaviour between individual grain boundaries. Significantly, many of the grain boundaries showing a weak PTC effect have low CSL Sigma (S) values(1). Previous workers have also noted that in undoped BaTiO3 there are around three times as many S = 3 grain boundaries as would be expected by chance(2).

In the current study the development of low S grain boundaries in a commercial Ca, Sr, Pb doped BaTiO3 PTC thermistor has been assessed through interrupted sintering experiments.

Electron Backscatter Pattern (EBSP) analysis was used to establish grain boundary misorientation distributions in a sintered thermistor puck, and in a series of samples prepared during an interrupted sintering study.

In the fully sintered sample a significant proportion of PTC inactive S=3 and S=9 boundaries were observed, S=3 boundaries being systematically preferred relative to other CSL indexable boundaries. Since these grain boundaries are believed to be PTC inactive, their presence is likely to be deleterious to the overall performance of a thermistor during switching.

Grain boundary orientation data from the interrupted sintering samples showed an increase in the proportion of coherent low energy S=3 boundaries with sintering time, occurring alongside a change in grain morphology from rounded to angular. The proportion of S=5 and S=9 boundaries, however, remained approximately constant during sintering. The implications of these observations on microstructural development and performance of PTC thermistors will be discussed.

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