Design of Interface Card in Telemetry Data Processing System

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Abstract

This paper introduces design principle of interface card used in PC-based telemetry data processing system. FPGA is adopted as the core device to implement I/O control and data buffering. The VHDL implementation of FPGA design is introduced. Some anti-interference measures are also discussed.

1 Introduction

PC-based telemetry data processing system accomplishes data reception, storage and processing tasks of two telemetry data streams. As the communication interface between PC and other ground telemetry equipments, the main function of data interface card is cooperating with processing software to implement the telemetry data buffering, timing data inserting and collection of AGC signal.

The main interface signals are shown in Fig.1.

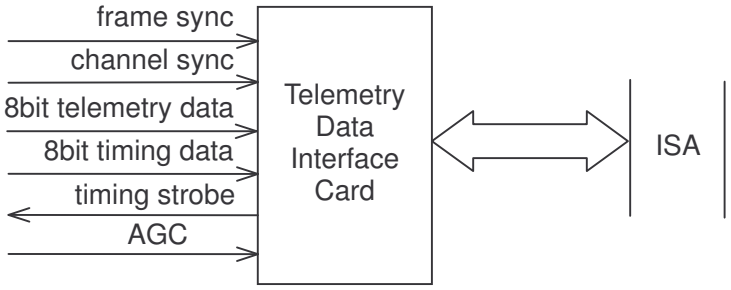

Fig.1 The main interface signals

Channel Sync: Input, from Demodulator, for the synchronous locking of telemetry data;

Frame Sync: Input, from Demodulator, indicating the initial position of telemetry frame;

Telemetry Data: Input, from Demodulator, 8bit parallel, alterable code rate up to 2Mbps;

Timing Data: Input, from Timer, five bytes BCD code (representative hour, minute, second, 0.01s, 0.0001s), locked by Frame Sync;

Timing Strobe Signal: Output, to Timer, five pulses per frame;

AGC: Input, from receiver, 0~5V, sampling resolution 8bit.

2 Design Principle

The 64k $\times$ 8 dual port RAM IDT7008 is adopted for data buffer. This device provides two independent ports (L-port and R-port) with separate control, address and I/O pins that permit

independent, asynchronous access for reads or writes to any location in memory. Its address range is 0~FFFFH. The new telemetry, timing and AGC sampling data are written into RAM via R-port. The L-port of RAM is mapped into memory space of computer. The connection of the highest bit of address lines is shown in Fig.2, which is controlled by ‘switch’ signal. In this way, 64kB address space is divided into two independent 32kB parts: Buffer A (0~7FFFH) and Buffer B (8000H~FFFFH). The two buffers can be accessed alternatively by computer or interface card itself.

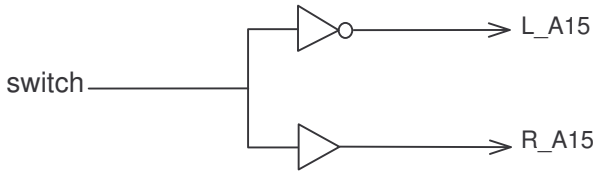

Fig.2 Partition and switch of data buffer

For example, once Buffer A is full of data (that is to say, the number of data frames is equal to the preset value), the level of ‘switch’ signal is changed to switch the access object of two buffers: Buffer A is mapped into PC’s memory space for data access, and Buffer B will be written in new data. At the same time, the interrupt signal occurs so as to notice the application of the buffer switch (namely data update) information.

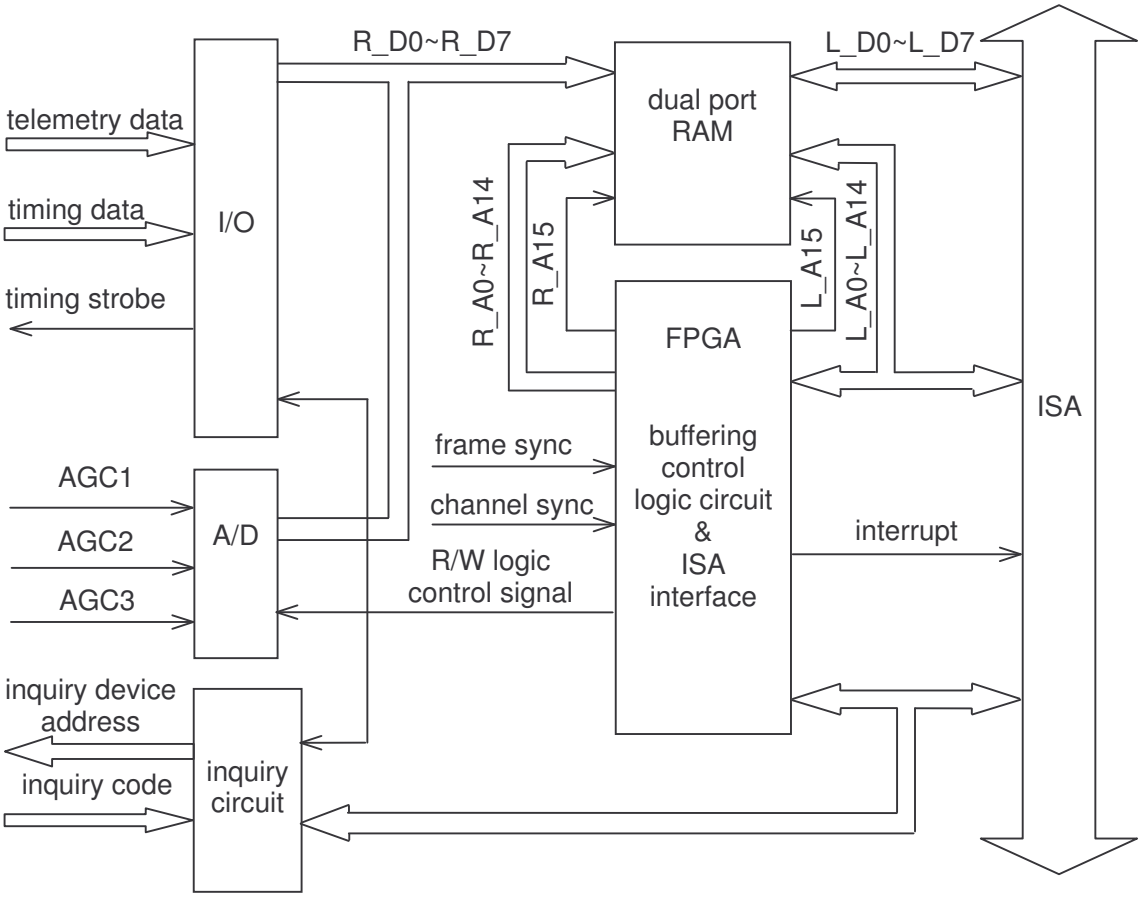

Fig.3 Function diagram of Data Interface Card

Telemetry Data Interface Card consists of dual port RAM, I/O interface, inquiry circuit, A/D converter (AGC sampling circuit) and FPGA (includes data buffering control logic and ISA interface circuit). The circuit function diagram is shown in Fig.3.

3 FPGA Design

FPGA is the core circuit of interface card. It is designed in VHDL. It adopts the methods of global asynchronous reset and clock synchronous timing design. Clock frequency is 20MHz. The main implementation function of FPGA includes ISA bus interface, I/O interface timing and dual port RAM R/W control.

3.1 ISA Bus Interface

Four I/O ports are assigned to interface card, respectively register of frame count, register of frame length (12bit, to occupy two I/O ports), register of command word and register of status word. Therein the registers of command word and status word share the same I/O port address: when executing I/OW instruction, as register of command word it accepts the commands that computer sends; when executing I/OR instruction, as register of status word it sends the status information to computer. The registers of frame count and frame length are used to setup the frame structure of telemetry data. The register of frame count is preset to the number of buffering frame, namely the capacity of data buffer. The register of frame length is directly correlated to the frame format of telemetry data, namely the bytes per frame, which also can be adjusted according to telemetry system and code rate.

3.2 I/O Interface Timing

There are three state machines in this design: state machine of frame sync, state machine of channel sync and state machine of channel count. The main function of state machine of frame sync is to judge the frame sync signal and send out frame sync pulse. The main function of state machine of channel sync is to judge the channel sync signal and divide channel period into several timing segments so as to implement the time-division buffering of telemetry, timing and AGC sampling data. The main function of state machine of channel count is to note the former several channel periods in a frame of telemetry data. The timing data is recorded in these five channel periods, and AGC sampling data is recorded in three channel periods.

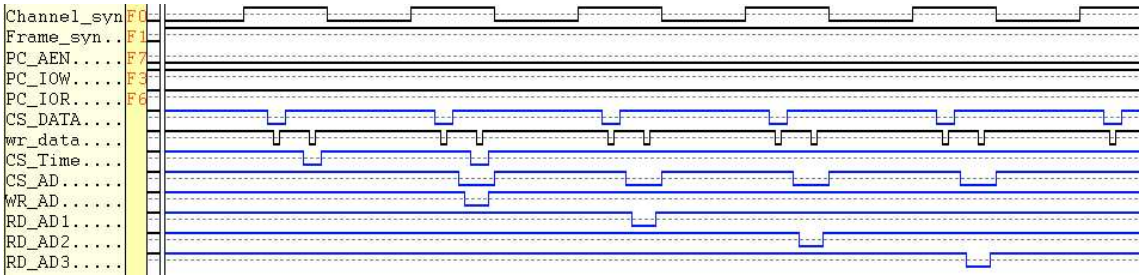

Fig.4 Simulation timing analysis of key R/W control

The simulation timing analysis of key R/W control signal is shown in Fig.4. ‘Channel_syn’ and ‘Frame_syn’ represent input frame sync and channel sync signals. ‘CS_DATA’, ‘CS_Time’

and ‘CS_AD’ are respectively the strobe signals of telemetry data, timing data and AGC sampling data. ‘wr_data’ is write operation signal of dual port RAM. In this way, the time-division data buffering is implemented.

The simulation timing analysis of buffering switch is shown in Fig.5. ‘INT’ is interrupt signal. ‘A15_L’ is the highest bit of L-port address lines of dual port RAM, and ‘A15_R’ is that of R-port. When the frame count goes back to zero, the two data buffers switch each other, namely ‘A15_L’ and ‘A15_R’ interchange. Also the interrupt occurs. After the computer responds to the interrupt signal and reads the status word (‘PC_IOR’ signal is low), the interrupt signal ‘INT’ is cleared.

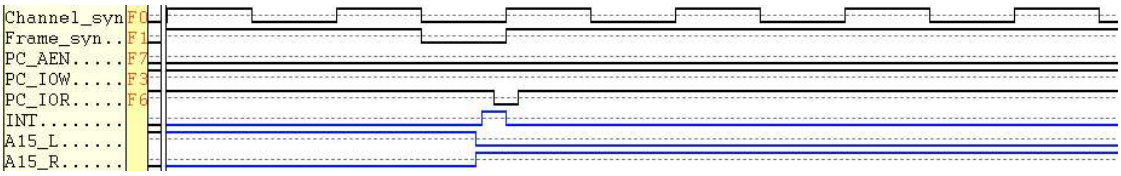

Fig.5 Simulation timing analysis of buffering switch

4 Anti-Interference Measures

Although some hardware anti-interference measures have been taken in circuit design, it is difficult to avoid from interference because of complexity and randomness of produced interference. So the technology of software anti-interference is necessary as additive means except for hardware anti-interference measures.

The technologies of software anti-interference such as digital filter, automatic verification in information transmission, system status monitoring and automatic recovery from failure are commonly used. The software anti-interference measures introduced in this paper are mostly implemented by VHDL design method.

4.1 Synchronization Design

The design of clock synchronous timing circuit is recommended for FPGA, which is helpful to enhance stability and anti-interference ability of system.

In the initial design, synchronous circuit is not adopted in the sampling of frame sync and channel sync signals, which results in the phenomena of data lost. After synchronous circuit design is adopted, the problem is resolved.

4.2 Information Verification

Automatic verification of important information can prevent interference and wrong action. For important information such as command word or status word, the methods of twice transmission or two bits repeat may be adopted.

4.3 State Machine Design

The design of state machine can also enhance anti-interference ability of system. For example, the positive-logic frame sync or channel sync signal is not valid unless the sampling signals in several continuous clock periods are always high so as to get rid of false signal.

4.4 I/O Read/Write

The control and information feedback of interface card are mainly implemented by I/O read/write, so should pay attention to its reliability. First of all, to verify the feedback information after I/OW operation is completed so as to ensure the written information correct. The second, to prevent incorrect change of frame count register and frame length register in the working process, ‘start’ signal is served as shutoff signal of writing operation, namely, writing operation of frame count register and frame length register is forbidden after interface card starts to work.

5 Conclusion

Telemetry data interface card is implemented with FPGA as core control unit and dual port RAM as data buffering unit. Hardware circuit is simplified, meanwhile, interface card has advantages of high reliability and flexibility. FPGA design adopts VHDL method, and takes some anti-interference measures. These measures are testified to be effective.